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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
08/822,962	03/21/97	KHORRAMABADI	R	PHA1306

D2M1/0313

US PHILIPS CORPORATION
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EXAMINER	
JEANPIERRE,P	
ART UNIT	**PAPER NUMBER**
2104	

DATE MAILED: 03/13/98

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/822,962	Applicant(s) Khorramabadi
	Examiner Peguy JeanPierre	Group Art Unit 2104

☒ Responsive to communication(s) filed on *Mar 21, 1997*.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-15* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-15* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *2/1 page*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

1. The drawings are objected to because of the following minor informalities:

In Figure 1 blocks 114, 116, 120, and 122 are not labeled.

In Figures 2 and 3 block 208 is not labeled. In addition, Figure 2 must be labeled "Prior Art". Moreover, there are no reference numerals for the 3 elements of path 212.

In Figure 11, block 1108 is not labeled.

In Figure 13, blocks 804, 218a, 804 b, and 218b are not labeled.

Correction is required.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 7, and 9-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patterson, III (USP 4,282,515) in view of Mangelsdorf (USP 5,436,629).

Patterson discloses in Figure 3 an analog to digital converter input (106) which is connected to an analog signal processing means (104). The system of Patterson further comprises of a compensation means which includes a first means (100) for fixing the level of the input signal, a second means (gain and offset correction 116, 118) which is connected to the output of the analog to digital converter input (106) for storing the output signal associated with the level, and a third means (D/A, Decoder 108) connected to the second means (118) for inputting the signal stored in (118) through buffer amplifier (150) to a modifying circuit (104). The modifying circuit

(104) further receives another input from an amplifier (102) and its output is connected to the analog to digital converter (106). However, Patterson fails to disclose the limitations of an analog to digital converter output.

Mangelsdorf discloses in Figure 1 an analog to digital converter which comprises of an adc input (20), a dac (22), and an adc output (28).The converters of Mangelsdorf are flash analog to digital converters which comprise a plurality of switches. It is known in the art of multistage flash analog to digital converter that the first stage produces the most significant bit and errors due to inaccuracies are reduced in the second stage, and both stages are combined to produce the digital output signal. Therefore, it would have been obvious to one having ordinary skill in the art to incorporate in the system of Patterson the analog to digital converter output as taught by Mangelsdorf to improve the accuracy of analog to digital converter.

4. Claims 5-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patterson, III (USP 4,282,515) and Mangelsdorf (USP 5,436,629) as applied to claims 1-3, 7, and 9-15 above, and further in view of Suarez-Garner (USP 3,906,488).

These claims add the limitations of a control logic circuit which controls a plurality of switches in accordance with the content of a signal stored in the register.

Suarez-Gartner discloses these limitations in Figure 2. The system comprises of an analog to digital converter (12) which is connected to a digital number storage means. The storage means is connected to control means for controlling the digital to analog switching circuit (see abstract). This technique is known in the art for decreasing the number of components. Therefore, a person

with working knowledge in the art would have been motivated by the time the invention was made to incorporate in the system of Patterson and Mangelsdorf the control logic as taught by Suarez-Gartner to reduce the circuit size so critical in wireless communication syatem.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sawai (USP 5,463,395) discloses a flash AD converter which employs a correction encoder for eliminating errors in the output signals.

Ryu (USP 5,426,431) discloses a converter in which a plurality of digital switches are controlled in accordance with the content of a register.

Matsuura et al. (USP 5,394,148) discoses a cascaded stage analog to digital converter.

Evans et al. (USP 4,590,458) disclose an offset removal in an analog to digital conversion system.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peguy JeanPierre whose telephone number is (703) 308-1968. Any inquiry of a general nature or related to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-1782.

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March 8, 1998

Howard L. Williams

HOWARD L. WILLIAMS
PRIMARY EXAMINER
GROUP 210